

**ABSTRACT OF THE DISCLOSURE**

A memory-efficient convolutional interleaver/de-interleaver with a memory array, a write commutator, and a read commutator wherein the commutators perform their respective write and read operations relative to a preselected memory cell after a  
5 predetermined delay. The delay is chosen using a modulo-based technique, such that an efficient implementation of a Ramsey Type-II interleaver is realized.